

CLAIMS:

What is claimed is:

1           1.    A method of generating carry information during an  
2 arithmetic operation of a first input signal A and second  
3 input signal B, the method comprising:

4           generating a plurality of carry-create signals in  
5 response to logical combinations of corresponding first groups  
6 of bit pairings of the first and second input signals;

7           generating a plurality of carry-transmit signals in  
8 response to logical combinations of corresponding second  
9 groups of bit pairings of the first and second input signals,  
10 wherein the first groups of bit pairings are different from  
11 the second groups of bit pairing; and

12           logically combining the carry-create and carry-transmit  
13 signals to create a number of accumulated carry-create signals  
14 that represent accumulated carry information at predetermined  
15 bit intervals.

1           2.    The method of Claim 1, wherein each carry-create  
2 signal is generated according to the logical expression  $J[z \rightarrow x]$   
3  $= (A_z | B_z) + (A_y | B_y) + (A_x | B_x)$ , where  $|$  is the logical AND  
4 operation and  $+$  is the logical OR operation, and  $x$ ,  $y$ , and  $z$   
5 represent consecutive bit positions of the input signals.

1           3.    The method of Claim 1, wherein each carry-transmit  
2 signal is generated according to the logic expression  $T[z \rightarrow x] =$   
3  $(A_z + B_z) | [(A_y + B_y) | (A_x + B_x) + (A_y | B_y)]$ , where  $|$  is the  
4 logical AND operation and  $+$  is the logical OR operation, and  
5  $x$ ,  $y$ , and  $z$  represent consecutive bit positions of the input  
6 signals.

1           4.    The method of Claim 1, wherein the logically  
2 combining step is implemented using carry look-ahead logic.

1           5.    The method of Claim 1, further comprising:  
2           generating a number of carry translation signals in  
3 response to logical combinations of corresponding third groups  
4 of bit pairings of the first and second input signals;  
5           generating a number of pairs of complementary pre-sum  
6 signals in response to a logical addition of the input  
7 signals;  
8           logically combining the carry translation signals with  
9 corresponding pairs of complementary pre-sum signals to  
10 generate a number of pairs of complementary sum signals; and  
11           selecting one from each pair of complementary sum signals  
12 in response to corresponding accumulated carry-create signals  
13 to generate a sum signal.

1           6.    The method of Claim 5, wherein each carry  
2 translation signal is generated according to the logical  
3 expression  $CT[y \rightarrow x] = (Ay + By) | (Ax + Bx) + (Ay | By)$ , where  $|$  is  
4 the logical AND operation and  $+$  is the logical OR operation,  
5 and  $x$  and  $y$  represent consecutive bit positions of the input  
6 signals.

1           7.    The method of Claim 1, further comprising:  
2           generating a number of carry translation signals in  
3 response to logical combinations of corresponding third groups  
4 of bit pairings of the first and second input signals;  
5           logically combining each of the carry translation signals  
6 with a corresponding accumulated carry-create signal to  
7 generate a number of accumulated carry-generate signals;  
8           generating a number of pairs of complementary sum signals  
9 in response to a logical addition of the input signals; and

10 selecting one from each pair of complementary sum signals  
 11 in response to corresponding accumulated carry-create signals  
 12 to generate a sum signal.

1 8. An adder for generating carry information during an  
 2 arithmetic operation of a first input signal A and second  
 3 input signal B, comprising:

4 means for generating a plurality of carry-create signals  
 5 in response to corresponding first groups of bit pairings of  
 6 the first and second input signals;

7 means for generating a plurality of carry-transmit  
 8 signals in response to corresponding second groups of bit  
 9 pairings of the first and second input signals, wherein the  
 10 first groups of bit pairings are different from the second  
 11 groups of bit pairings;

12 means for logically combining the carry-create and carry-  
 13 transmit signals to create a number of accumulated carry-  
 14 create signals that represent accumulated carry information at  
 15 predetermined bit intervals.

1 9. The adder of Claim 8, wherein the means for  
 2 generating the carry-create signal has a stack height of two.

1 10. The adder of Claim 8, wherein the means for  
 2 generating the carry-create signal comprises a logic circuit  
 3 configured to implement the logical expression  $J[z \rightarrow x] =$   
 4  $(A_z | B_z) + (A_y | B_y) + (A_x | B_x)$ , where  $|$  is the logical AND  
 5 operation and  $+$  is the logical OR operation, and  $x$ ,  $y$ , and  $z$   
 6 represent consecutive bit positions of the input signals.

1 11. The adder of Claim 8, wherein the means for  
 2 generating the carry-transmit signal has a stack height of  
 3 three.

1           12. The adder of Claim 8, wherein the means for  
2 generating the carry-transmit signal comprises a logic circuit  
3 configured to implement the logical expression  $T[z \rightarrow x] = (Az +$   
4  $Bz) \mid [(Ay + By) \mid (Ax + Bx) + (Ay \mid By)]$ , where  $\mid$  is the logical  
5 AND operation and  $+$  is the logical OR operation, and  $x$ ,  $y$ , and  
6  $z$  represent consecutive bit positions of the input signals.

1           13. The adder of Claim 8, wherein the means for  
2 combining comprises carry look-ahead logic.

1           14. The adder of Claim 8, further comprising:  
2 means for generating a number of carry translation  
3 signals in response to logical combinations of corresponding  
4 third groups of bit pairings of the first and second input  
5 signals;  
6 means for generating a number of pairs of complementary  
7 pre-sum signals in response to a logical addition of the input  
8 signals;  
9 means for logically combining the carry translation  
10 signals with corresponding pairs of complementary pre-sum  
11 signals to generate a number of pairs of complementary sum  
12 signals; and  
13 means for selecting one from each pair of complementary  
14 sum signals in response to corresponding accumulated carry-  
15 create signals to generate a sum signal.

1           15. The adder of Claim 14, wherein the means for  
2 generating the carry translation signal comprises a logic  
3 circuit configured to implement the logical expression  $CT[y \rightarrow x]$   
4  $= (Ay + By) \mid (Ax + Bx) + (Ay \mid By)$ , where  $\mid$  is the logical AND  
5 operation and  $+$  is the logical OR operation, and  $x$  and  $y$   
6 represent consecutive bit positions of the input signals.

16. The adder of Claim 8, further comprising:  
 means for generating a number of carry translation signals in response to logical combinations of corresponding third groups of bit pairings of the first and second input signals;  
 means for logically combining each of the carry translation signals with a corresponding accumulated carry-create signal to generate a number of accumulated carry-generate signals;  
 means for generating a number of pairs of complementary sum signals in response to a logical addition of the input signals; and  
 means for selecting one from each pair of complementary sum signals in response to corresponding accumulated carry-create signals to generate a sum signal.

17. An adder for generating carry information during an arithmetic operation of a first input signal A and second input signal B, comprising:

a plurality of carry-create circuits, each for generating a carry-create signal J in response to corresponding bit pairings of the input signals according to the logical expression  $J[z \rightarrow x] = (A_z | B_z) + (A_y | B_y) + (A_x | B_x)$ , where  $|$  is the logical AND operation,  $+$  is the logical OR operation, and x, y, and z represent consecutive bit positions of the input signals;

a plurality of carry-transmit circuits, each for generating a carry-transmit signal T in response to corresponding bit pairings of the input signals according to the logical expression  $T[z \rightarrow x] = (A_z + B_z) | [(A_y + B_y) | (A_x + B_x) + (A_y | B_y)]$ ; and

carry look-ahead logic for logically combining the carry-create signals and the carry-transmit signals to generate a

18 number of accumulated carry-create signals that represent  
19 accumulated carry information at predetermined bit intervals.

1 18. The adder of Claim 17, further comprising:  
2 a plurality of carry translation circuits, each for  
3 generating a carry translate signal CT in response to  
4 corresponding bit pairings of the input signals according to  
5 the logical expression  $CT[y \rightarrow x] = (A_y + B_y) | (A_x + B_x) +$   
6  $(A_y | B_y)$ .

1 19. The adder of Claim 18, where the carry-translate  
2 circuit is incorporated within the carry-transmit circuit.

1 20. The adder of Claim 18, further including a number of  
2 sum generators, each comprising:

3 a sum circuit for generating pairs of complementary pre-  
4 sum bits in response to logical additions of corresponding  
5 bits of the input signals;

6 translation logic having inputs to receive the pairs of  
7 complementary pre-sum signals, an input to receive a  
8 corresponding carry-translation signal, and outputs to provide  
9 pairs of complementary sum bits; and

10 a multiplexer having inputs to receive the pairs of  
11 complementary sum bits, a select terminal to receive a  
12 corresponding accumulated carry-create signal, and an output  
13 to provide corresponding bits of a sum signal.

1 21. The adder of Claim 20, wherein the translation logic  
2 translates pairs of complementary pre-sum bits into  
3 corresponding pairs of complementary sum bits.

1 22. The adder of Claim 20, wherein each sum generator  
2 generates the sum bits  $S[5:3]$  according to the logical

3 expression  $S[5:3] = J[2 \rightarrow 0] \mid CT[2 \rightarrow 1] \mid SUM1[5:3] +$   
 4  $JB[2 \rightarrow 0] \mid CTB[2 \rightarrow 1] \mid SUM0[5:3]$ , where  $JB[2 \rightarrow 0] = \overline{A_2} \mid \overline{B_2} + \overline{A_1} \mid \overline{B_1} +$   
 5  $\overline{A_0} + \overline{B_0}$ ,  $CTB[2 \rightarrow 1] = (\overline{A_2} + \overline{B_2}) \mid (\overline{A_1} + \overline{B_1}) + \overline{A_2} \mid \overline{B_2}$ , and  $SUM1[5:3]$   
 6 and  $SUM0[5:3]$  are pairs of complementary sum bits.

1 23. The adder of Claim 17, wherein each carry-create  
 2 circuit has a stack height of two.

1 24. The adder of Claim 17, wherein each carry-create  
 2 circuit comprises:

3 first and second transistors connected in series between  
 4 an output and a first node, the first transistor responsive to  
 5  $A_x$ , the second transistor responsive to  $B_x$ ;

6 third and fourth transistors connected in series between  
 7 the output and the first node, the third transistor responsive  
 8 to  $A_y$ , the fourth transistor responsive to  $B_y$ ; and

9 fifth and sixth transistors connected in series between  
 10 the output and the first node, the fifth transistor responsive  
 11 to  $A_z$ , the sixth transistor responsive to  $B_z$ .

1 25. The adder of Claim 17, wherein each carry-create  
 2 circuit further comprises:

3 a PMOS pull-up transistor coupled between a supply  
 4 voltage and the output, the pull-up transistor responsive to a  
 5 clock signal; and

6 an NMOS pull-down transistor coupled between the first  
 7 node and ground potential, the pull-down transistor responsive  
 8 to a complement of the clock signal.

1 26. The adder of Claim 17, wherein each carry-transmit  
 2 circuit has a stack height of three.

1           27. The adder of Claim 17, wherein each carry-transmit  
2 circuit comprises:

3           first and second transistors connected in parallel  
4 between an output and a first node, the first transistor  
5 responsive to Az, the second transistor responsive to Bz;

6           third and fourth transistors connected in series between  
7 the first node and a second node, the third transistor  
8 responsive to Ay, the fourth transistor responsive to By;

9           fifth and sixth transistors connected in parallel between  
10 the first node and a third node, the fifth transistor  
11 responsive to Ay, the sixth transistor responsive to By; and

12           seventh and eighth transistors connected in parallel  
13 between the third node and the second node, the sixth  
14 transistor responsive to Ax, the seventh transistor responsive  
15 to Bx.

1           28. The adder of Claim 17, wherein each carry-transmit  
2 circuit further comprises:

3           a PMOS pull-up transistor coupled between a supply  
4 voltage and the output, the pull-up transistor responsive to a  
5 clock signal; and

6           an NMOS pull-down transistor coupled between the second  
7 node and ground potential, the pull-down transistor responsive  
8 to a complement of the clock signal.